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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/552,761	04/18/2000	Stefan Eckart	0100.0000550	3105

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EXAMINER

REKSTAD, ERICK J

ART UNIT	PAPER NUMBER
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2613

DATE MAILED: 08/03/2004

12

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/552,761

Applicant(s)

ECKART, STEFAN

Examiner

Erick Rekstad

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 May 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5 and 27 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-8, 11-25, 28 and 29 is/are rejected.
- 7) ☐ Claim(s) 9, 10 and 26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This action is in response to applicants request for continued examination for application no. 09/552,761 in which claims 1-29 are presented for examination.

Response to Arguments

Regarding the argument on pages 11-17 of the RCE filed March 10, 2004 applicant asserts that not all of the limitations of claims 1 and 2 are met by Uz. Again to explain the examiner's interpretation of Uz, a first Q will produce x bits for the I frame (it does not vary for this given number of frames). Then if Q should be varied, the bit rate will change for at least the next frame. The interpretation of the claims' statement "number of frames" is one frame. Therefore, Uz satisfies the requirements of the claim.

Regarding the applicant's arguments on pages 17-18 related to claim 3. As cited in the Office Action, TA was equated to meet the power limitation. Applicant's own specs (page 27) appears to teach that power is fully based on complexity. Thus, the TA appears to meet the power limitation.

Regarding the arguments on pages 18-19 regarding claims 6-8, and 24. Applicant argues that the limitation of "calculating a sum of absolute values of the pixel level error values for a pixel block" is not met by Uz. Applicant sites Col. 9 Lines 22-28 but does not address Section B (Col.8 Lines 51-54) referred to in the previous Office Action as showing that the error is related to absolute differences. Applicant argues that the expected number of bits does not equate to the intra/inter selection. However, given that IB (Intra-bias) is a function of IA (Intra-activity) and Q (quantization scale factor) which is a number of assigned values (bits). The number of bits is compared to

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thresholds to determine inter/intra coding. Thus, the limitations of claims 6,7,8, and 24 are considered met by Uz.

According to the arguments on page 19-20, relevant to claims 11,12,13 and 14, the applicant argues that the examiner has not shown the prediction of a relationship between a quantizer scale factor and a number of encoded bits of a pixel block based on a known relationship in previous pixel blocks of a same type. The predicted relationship is shown by Uz on Col. 11 Line 60-Col. 12 Line 9, where the rate control quantization scale factor is based on the bit budget and complexity (TA). The applicant states complexity as an example of a known relationship (page 11). Uz further uses the initial value of Q to determine initial occupancies for the corresponding virtual buffers. These virtual buffers are then used to provide a mechanism to relate the number of bits allocated to a macroblock and the quantization scale factor selected for the macroblock (Col. 13 Lines 17-30). Thus, the limitations of claims 11, 12, 13 and 14 are considered met by Uz.

In response to applicant's arguments on page 20-22, related to claims 15-18, the applicant states Uz does not teach the step of "using the group of pictures level predicting, the picture level predicting, and the pixel block-level predicting to adjust a quantizer scale factor". To clarify the examiner's position, please note Col 11 lines 40-49 where Uz teaches the calculation of a group of picture level prediction for a number of bits. Uz calculates a picture-level for a number of bits on Col. 12 lines 49-55. Uz calculates a pixel-block-level on Col. 12 lines 56-65. Uz then uses the number of bits to determine the quantization factor (Col. 13 Lines 17-30). The number of bits for each

stage are obtained from the values from the previous stage, thus the final quantization factor is based on all three of the stages. To further clarify the examiner's position, the GOP level is viewed as being calculated as it is based on the intra-activity and VBV occupancy. The intra-activity and VBV occupancy are obtained through calculations (Col 9 Lines 22-43, Col 13 Lines 61-63). Uz further satisfies claim 16 with the calculation of picture-level prediction. The calculation is based on block type, the sum of absolute values of pixel-level error values (Col 9 Lines 8-10) and a pixel block complexity. The pixel block complexity (TA) is based on the absolute differences. Applicant further argues the use of (TA) for two presumed completely different parameters. As suggested by the examiner above, the TA is the power for claim 3 as provided by the specs and is also a value of block complexity. Therefore as best understood by the examiner, power value is equivalent to pixel block complexity.

As for claim 19, the applicant argues that the scene prediction of UZ is not based on a prediction error image. Uz uses the sum of the absolute differences of the pixels in the macroblocks and the corresponding pixels in the prediction of the macroblocks in the reference frame (Col. 11 Lines 22-32). As best understood by the examiner, the differences calculated would produce a prediction error image. Uz then adds up the macroblocks in the error image to determine scene change. Thus, the limitations of claim 19 are met by Uz.

Regarding claim 4, Applicant's arguments have been considered but are moot under the new grounds of rejection.

Regarding arguments on page 27 related to claims 21 and 22. Applicant has not addressed the rejection as found in the previous Office Action dated Feb. 9, 2004. As stated in that Office Action, Uz teaches in figure 1a, the apparatus for rate control for a constant-bit-rate finite-buffer-size video encoder comprising a preprocessing stage (20) for determining a power value (TA) (Col 8 Lines 32-67, Col 9 Lines 1-10) and a group-of-pictures-level rate control block (30) operatively coupled to the preprocessing stage to receive the power value and to provide a target quantizer step size used to provide rate control for the video encoder (Col. 11 Lines 12-67 and Col. 12 Lines 1-9). Therefore Uz satisfies the requirements of claim 21. Further, Uz teaches the updating of the power value for each subsequent picture being encoded (Col. 8 Lines 33-35). Claim 23 is further satisfied as Uz teaches the non-intra frames having sizes based on the expected size of the future intra frames (Col. 11 Lines 41-49).

As for claim 20, applicant argues that Kuchibhotla does not teach the required steps to satisfy claim 20. To clarify the examiners position, please take note of Col 3 Line 53-Col 4 line 5. Kuchibhotla teaches counting the total intra-coded macroblocks and comparing the count to a threshold level. The threshold level is obviously based on the desired number of intra coded blocks in the total number of macroblocks. Inversely, this would be the desired number of inter coded blocks in the total number of macroblocks. The comparison between the number of intra-coded blocks and the number of total macroblocks is equivalent to taking the ratio of intra-to-inter blocks and comparing the ratio to a threshold.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 28 and 29 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by US Patent 5,241,383 to Chen et al.

[claims 1 and 28]

Chen teaches a method for rate control for a constant-bit-rate finite-buffer-size video encoder comprising the steps of:

Calculating a first quantizer step size such that a first number of bits generated at an output of the constant-bit-rate finite-buffer-size video encoder is constant over a first given number of frames (SGOP) starting at a current frame;

Incrementing the current frame (to next SGOP); and

Calculating a second quantizer step size such that a second number of bits generated at the output of the constant-bit-rate finite-buffer-size video encoder is constant over a second given number of frames starting at the incremented current frame (Abstract, Col 3 Lines 52-56, Col 5 Lines 28-31, Col 10 Lines 20-51, Col 12 Lines 3-22). Chen further teaches the quantizer is obtained in a single pass as required by claim 28 (Col 10 Lines 20-30).

[claim 2 and 29]

Chen teaches using a second given number of frames that is equal to the first given number of frames (Col 1 Lines 41-42).

Claims 1-3,6-8, 11-19 and 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5,686,963 to Uz et al.

[claim 1]

Uz teaches the use of a quantizer step size to control the number of bits used to encode each macroblock (Col 2 Lines 52-58). Uz also states that by adjusting the quantization step size the bits for a frame in a GOP can be set (Col 12 Lines 4-9). It is clear that the quantizer step size (Q_n) can be calculated such that a first number of bits generated at an output of the constant-bit-rate finite-buffer-size video encoder is constant over a first given number of frames (GOP) starting at a current frame and that the quantizer step size can be calculated for a second given number of frames (Col 12 Lines 56-60). Note Col. 11 Lines 40-47, where an initial quantizer step (default) will allow for x bits to be distributed over an I frame, (or P or B). This meets the limitation of a first quantizer step for a fixed rate over a first given number of frames. Then in Col. 11 Lines 60- Col. 12 Line 6 a new quantization scale is calculated for a new given number of frames (be it I, P or B) and continues to update.

[claim 2]

Uz use of the quantization stepsize to adjust the bits for a frame in a GOP clearly shows that the quantization stepsize can be calculated over a GOP and then calculated again for a GOP of the same size (Col 1 Lines 50-51,Col 12).

[claim 3]

Uz teaches calculating a power value (total activity (TA)) for each frame that is used to change the rate control quantization scale factor (Col 11 Lines 61-66).

Adjusting a number of bits in a second frame based on the power value (TA) for the first frame is achieved by using the rate control quantization scale factor (Col 12 Lines 49-55). Note, TA was equated to meet the power limitation. Applicant's own specs (page 27) appears to teach that power is fully based on complexity. Thus, the TA appears to meet the power limitation.

[claims 6,7,8 and 24]

Uz describes obtaining a prediction error frame (motion compensated prediction) including a plurality of pixel-level error values (subtracting the motion compensated prediction of a macroblock from the macroblock to be encoded) (Col 9 Lines 23-27). A calculated sum of absolute values of the pixel-level error values for a pixel block is obtained (displaced frame difference activity (DPDA) (Col 9 Lines 23-27). A calculation of an expected number of bits for the pixel block based on the sum of the absolute values (DFDA) is done by the function to determine if a macroblock should be inter or intra coded (Col 9 Lines 38-42). The expected number of bits for a block, frame and GOP are calculated (Bit Budget) and used to obtain constant-bit-rate video encoding (Col 12).

[claims 11-14]

Uz describes a method of predicting a relationship between a quantizer scale factor and a number of encoded bits of a pixel block based on a known relationship in

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previous pixel blocks of a same type and using the quantizer scale factor to control a pixel block level rate (Col 12 Lines 56-67, Col 13 Lines 3-9).

[claims 15-18]

Uz describes calculating a group-of-picture-level and picture-level predictions for a number of bits encoded for a group of pictures (Col 11 Lines 42-49). The variable TA is dependent on the total activity of all the macroblocks and because the picture-level determination for number of bits is based on the TA variable and the TA is dependent on total activity of macroblocks, the determination is then a prediction at the pixel-block-level (Col 8 Lines 65-67, Col 9 Lines 8-10). Calculating the picture-level prediction for the number of bits encoded for the picture is based on a pixel block type (Col 12), a sum of absolute values of pixel-level error values (Col 11 Line 25) and a pixel block complexity (TA). Calculating the group-of-pictures-level prediction for the number of bits encoded for the group-of-pictures is based on a global complexity value (Reff, Col 12). The quantizer scale factor is adjusted based on the three predictions (Col 11 Lines 60-66).

[claim 19]

Uz describes the detection of a scene change using a prediction error image and using the scene change to reset the global complexity history TAI. TAI is used to provide the rate control for the video encoder (Col 11 Lines 10-55).

[claims 21-23]

Uz teaches in figure 1a, the apparatus for rate control for a constant-bit-rate finite-buffer-size video encoder comprising a preprocessing stage (20) for determining a

power value (TA) (Col 8 Lines 32-67, Col 9 Lines 1-10) and a group-of-pictures-level rate control block (30) operatively coupled to the preprocessing stage to receive the power value and to provide a target quantizer step size used to provide rate control for the video encoder (Col. 11 Lines 12-67 and Col. 12 Lines 1-9). Therefore Uz satisfies the requirements of claim 21. Further, Uz teaches the updating of the power value for each subsequent picture being encoded as required by claim 22 (Col. 8 Lines 33-35). Claim 23 is further satisfied as Uz teaches the non-intra frames having sizes based on the expected size of the future intra frames (Col. 11 Lines 41-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uz as applied to claim 3 above, and further in view of US Patent 6,226,326 to Mihara.

[claim 4]

Uz's TA variable is a sum of the total activities (sum of the absolute differences of pixel blocks) for all the macroblocks in a frame (Col 8 Lines 51-64). The controller maintains an average TA for the frames of a scene (Col 11 Lines 17-18). Uz does not teach how to calculate the average. Mihara teaches the steps for calculating the power value by calculating a sum of absolute differences between the pixel values in the

respective pixel block and the average value. The values are added for each of the plurality of pixel blocks within the first frame to obtain a power value for the first frame (Col 19, Lines 10-20). It would have been obvious to one skilled in the art at the time of the invention to calculate the average for each block or each frame as as taught by Mihara in order to obtain the energy value of the frame.

Claims 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uz in view of US Patent 5,724,100 to Kuchibhotla.

[claim 20]

Uz teaches the use of a method for rate control that obtains a scene change indication from a prediction error image and using the scene change indication to reset a global complexity history and using the global complexity history to provide the rate control for the video encoder. Uz does not teach the method of counting a first number of intra coded pixel blocks in the prediction error image, counting a second number of non-intra coded pixel blocks in the prediction error image, calculating a ratio of the first number and the second number, comparing the ratio to a threshold to determine a result and using the result as a scene change indication. Kuchibhotla does teach this method as a means to prevent exceeding a coding bit budget (Col 2 Lines 35-58, Col 3 Line 53-Col 4 line 5). It would have been obvious to one skilled in the art at the time of the invention to use the method of Uz in conjunction with the method of Kuchibhotla in order to prevent exceeding a coding bit budget.

[claim 25]

Uz teaches the calculation of complexity values for non-intra pixels and intra pixels (Col. 8 Lines 51-67 and Col. 9 Lines 1-5). Although Uz fails to teach the determining of intra vs non-intra blocks, Kuchibhotla does teach the determining of intra vs non-intra blocks (Fig. 1 element 134, Col 3 Line 30-Col 4 Line 5). Kuchibhotla further teaches the benefit of half-pel motion estimation to obtain a correct scene change detection (Col 4 Line 64-Col 5 Line 10). Since both systems provide constant-bit-rate it would have been obvious to one skilled in the art at the time of the invention to substitute Kuchibhotla's scene change detector into Uz's system since the scene change detector of Kuchibhotla has the advantage of accurately detecting scene change for half pixel motion compensation.

Allowable Subject Matter

Claims 5 and 27 are allowed.

Claims 9, 10 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6,507,615 to Tsujii et al.

US Patent 6,614,942 to Meier.

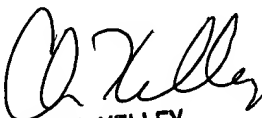
US Patent 5,038,209 to Hang.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erick Rekstad whose telephone number is 703-305-5543. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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